machine 210 and a pattern generator 230. The LBIST domain 160 also includes a **m**ultiple **i**nput **s**ignature **r**egister ("MISR") 220. The content of the MISR 220 is the LBIST signature 130 in **FIG. 1**. The pattern generator 230 is, more precisely, a **p**seudo **r**andom **p**attern **g**enerator ("PRPG"). In the illustrated embodiment, the LBIST engine 110 is externally configured by a CONFIGURATION signal with a vector count and a PRPG seed for the pattern generator 230. The LBIST engine 110 is configured by a 66-bit signal received through the testing interface 180 in which 32 bits contain the vector count and 33 bits contain the PRPG seed. Thus, the pattern generator 230 is programmable, as is the LBIST engine 110 as a whole. However, the invention is not so limited and other techniques may be employed for configuring the LBIST engine 110. For instance, these values may be hardcoded or hardwired in alternative embodiments.

In the illustrated embodiment, the LBIST engine 110 is also provided with the scan chain length in the ASIC 150. The value is, in this particular embodiment, hardwired to a value greater than the longest scan chain length in the ASIC 150. This value may be different for each implementation of the ASIC 150 and may be hard coded by the ASIC vendor. Furthermore, in some alternative embodiments, this value may be provided to the LBIST engine 110 through the testing interface 180.

Turning now to **FIG. 3**, the LBIST state machine 210 has five primary states: a reset state 310, an initialization state 320, a scan state 330, a step state 340, and a done state 350. The LBIST state machine 210 is reset, *i.e.*, transitions to the reset state 310, whenever an external reset signal is asserted regardless of which state in which it might be. On transition to the reset state 310, the MISR 220 and the pattern generator 230 are initialized. The LBIST state machine 210 remains in the reset state 310 until the LBIST RUN signal is received, whereupon it transitions to the initiate state 320. In the initiate state 320, the LBIST initiates the various signals to be used in the LBIST. For instance, the COUNTER(S), COMPLETE, and ERROR signals, whose functions shall be discussed more fully below, are initialized. The LBIST state machine 210 then automatically transitions to the scan state 330 and begins to repeatedly cycle through the scan state 330 and the step state 340. Note that, in the early cycles, the scan state 340 flushes the scan chains (not shown) and the MISR 220 is not loaded, in the illustrated invention, until after the scan chains flush.

The scan state 330 and the step state 340, together, comprise the actual LBIST. The LBIST state machine 210 cycles through the scan state 330 and the step state 340 until reset by the external reset signal or until the LBIST is complete. The LBIST can be performed repeatedly without resetting through the external reset signal. Prior to entering the done state 350, the LBIST state machine 210 cycles through the scan state 330 and the step state 340 a number of times based on the vector count. As mentioned above, in the illustrated embodiment, the vector count is externally configured. The LBIST state machine 210 of the illustrated embodiments cycles through the scan state 330 and the step state 340 until the content of the pattern generator 230 is equal to the vector count. However, alternative embodiments may base the number of cycles on the vector count in alternative manners.

If the LBIST completes without being externally reset, the LBIST state machine 210 transitions to the done state 350. In the done state 350, the LBIST engine 110 provides a "BIST complete" indicator signal COMPLETE. The COMPLETE indicator signal also indicates that the results are "fresh," *i.e.*, from the current LBIST and not from an old run. In accordance with one aspect of the present invention, the indicator signal COMPLETE sets a designated bit in the MISR 220 to indicate that the LBIST is complete in the LBIST signature 130. Thus, the LBIST signature 130 includes an indication of whether the LBIST is done. The LBIST engine 110 also provides an error signal ERROR, indicating the pattern generator 230 went to an "all zeros state," which is highly undesirable. Also in accordance with one aspect of the present invention, the ERROR signal sets a designated bit in the MISR 220 to indicate in the LBIST signature 130 that this error condition arose during the LBIST. Note that alternative embodiments of the present invention may omit one or both of the "done" and "error" indications in the LBIST signature 130 should they choose not to implement these aspects of the present invention.

The MISR 220 is, in the illustrated embodiment, a 32-bit register shown in **FIG. 4**. The MISR 220 is initialized when the LBIST state machine 210 resets and shifts during the scans. The MISR 220 may be implemented using any techniques known to the art. However, as was mentioned above, in the illustrated embodiment, one bit, *e.g.*, the bit B_{32}, is used to indicate that the LBIST is done/fresh and one bit, *e.g.*, the bit B_{33}, is used to indicate that an error condition arose. Furthermore, in accordance with yet another aspect of the present invention, the done bit of the MISR 220, *e.g.*, the bit B_{32}, is used to indicate that the

LBIST signature 130 stored in the MISR 220 is new or valid, and not the result of a previous run. For instance, this bit may be cleared when the LBIST state machine 210 enters the reset stage 310 and the MISR 220 is initiated, and then set when the LBIST state machine 210 enters the done state 350. Note that the MISR 220 can be implemented using registers having sizes other than 32 bits. The logic pattern held in the bits B_{31}-B_0 in the MISR 220 can then be externally compared to a known pattern after the LBIST is done to establish pass/fail results.

The pattern generator 230 is implemented, in the illustrated embodiment, in a 31-bit linear feedback shift register ("LFSR"), shown in **FIG. 5**, such as is known to the art. the pattern generator 230 may be implemented using any suitable technique known to the art. However, in the illustrated embodiment, the pattern generator 230 is initialized to the externally configured PRPG seed when the LBIST state machine 210 enters the reset state 310. Selected outputs of the LFSR supply the scan pattern to the inputs of the scan chains (not shown) in a conventional fashion. During scan, the LFSR continuously shifts from the most significant bit ("MSB") B_{30} to the least significant bit ("LSB") B_0.

In accordance with yet another aspect of the invention, the content of the LFSR with which the pattern generator 230 is implemented and the register with which the MISR 220 is implemented are generated using different primitive polynomials to prevent failures disguised by aliasing. The content of the LFSR in the illustrated embodiment is based on the 31-bit primitive polynomial $x^{31} + x^3 + 1$ and the content of the MISR 220 is based on the 32-bit primitive polynomial $x^{32} + x^{28} + x + 1$. If the pattern generator 230 enters an all zero state, the error indicator will be activated and stored in bit B_{33} of the MISR 220. In this particular embodiment, the even outputs of the LFSR (bits B_{26} to B_0) supply the scan pattern to the inputs of the scan chains 1 to 23, respectively. The MISR 220 has inputs that EXCLUSIVE-OR into the odd register bits B_7 through B_{31} and bit B_0 during the scan operation. Alternative embodiments may omit this aspect of the invention, however.

The LBIST engine 110 provides two level sensitive scan device ("LSSD") clock signals, shown in **FIG. 9**, to the level sensitive scan devices (not shown) in the core 900. Both of these clock signals are normally low, but alternately pulse high when the LBIST state machine 210 is in the scan state 330. After the scan chains are flushed, the MISR 220 (shown in **FIG. 2**) collects the scan data. The LBIST engine 110 also outputs two step clock signals